IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#5 B Tucker 1/28/03

Art Unit 2154
Examiner Larry D. Donaghue

In Re:	Mario D. Nemirovsky et al.
Case:	P3803
Serial No.:	09/312,302
Filed:	May 14, 1999
Subject:	**Interrupt and Exception Handling for Multi-Streaming Digital Processors**

To: The Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir;

Response A

All of the claims standing for examination are presented below for examination. No amendments to the claims or specification are herein made in the present response.

1. A multi-streaming processor system comprising:

a plurality of streams for streaming one or more instruction threads;

a set of functional resources for processing instructions from streams; and

interrupt logic;

wherein through the interrupt logic specific interrupts or exceptions are detected and mapped to one or more specific streams.

2. The system of claim 1 wherein one interrupt or exception may be mapped to two or more streams.